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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,537	07/22/2003	Yuji Yamamoto	107156-00194	4884

7590 01/12/2007

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EXAMINER	
DO, CHAT C	
ART UNIT	PAPER NUMBER
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/623,537	YAMAMOTO, YUJI	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2003 and 19 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/19/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because the abstract is written more than 150 words in length. Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities:

The applicant is advised to update information cited under the "Background of the invention" page 1 lines 8-11.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the necessary structure for requiring to appends as many bits as a shortfall to the LSB to generate a second bit string.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 1-15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-15 cite a transformer and its corresponding method of computing a logarithmic of an input. In order for claims to be statutory, claims must either include a practical/physical application or a concrete, useful, and tangible result. However, claims 1-15 merely disclose steps of computing the logarithmic of an input without disclosing the practical application or a tangible result. Therefore, claims 1-15 are directed to a non-statutory subject matter.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-6, 9, and 11-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Allred (U.S. 6,289,367).

Re claim 1, Allred discloses in Figures 4 and 6 a logarithmic transformer (e.g. abstract and either Figure 4 or 6 wherein the $\log_2(x)$ is logarithmic of input x) comprising: a first bit string generator for generating a first bit string of binary data indicating the position of a highest order bit of logic "1" out of bits of digital data to be logarithmically transformed (e.g. output of MSD identifier circuit 104); and a second bit string generator for determining, from digital data, a second bit string of order lower than highest order bit of logic "1" (e.g. r output of circuit 102 in Figure 4), the logarithmic transformer outputting logarithmic transformation data (e.g. ouput of 110 as logarithmic of input x), which includes first bit string as an integral part of a logarithmic transformation value resulting from a logarithmic transformation of digital data and second bit string as a fractional part of logarithmic transformation value (e.g. col. 5 lines 10-62).

Re claim 2, Allred further discloses in Figures 4 and 6 first bit string generator comprises: a detecting unit for detecting the position of highest order bit of logic "1" out of the bits of digital data; and a generating unit for generating first bit string based on a result of detection by detecting unit (e.g. MSD identifier circuit 104 in Figure 4).

Re claim 3, Allred further discloses in Figures 4 and 6 detecting unit detects highest order bit of logic "1" by decoding digital data (e.g. col. 8 lines 2-9 and col. 6 lines 18-50).

Re claim 4, Allred further discloses in Figures 4 and 6 generating unit contains pieces of binary data indicating the positions of the respective bits of digital data, and selects one out of pieces of binary data based on the result of detection by detecting unit, thereby generating binary data indicating the position of highest order bit of logic "1" (e.g. n as binary representation of MSD as integer of the logarithm as seen in Figure 4 and col. 8 lines 2-9).

Re claim 5, Allred further discloses in Figures 4 and 6 generating unit is composed of a switching circuit for selecting one out of pieces of binary data, based on the result of detection by detecting unit (e.g. col. 6 lines 10-32).

Re claim 6, Allred further discloses in Figures 4 and 6 detecting unit comprises: a first logic circuit for outputting data for excluding a bit string lower than highest order bit of logic "1" from the bits of digital data; and a second logic circuit for removing the bit string excluded by data from the bits of digital data, thereby detecting highest order bit of logic "1" (e.g. col. 6 lines 10-32).

Re claim 9, Allred further discloses in Figures 4 and 6 second bit string generator determines, as second bit string, a bit string of a predetermined number of bits including a bit following highest order bit of logic "1" out of the bits of digital data (e.g. r as second bit string in Figure 4 as output of component 102)..

Re claim 11, Allred further discloses in Figures 4 and 6 second bit string generator comprises: a second bit string extracting unit for inputting digital data as successive bit strings each having predetermined number of bits; and a second bit string selecting unit for making second bit string extracting unit to extract, as second bit string, a bit string of predetermined number of bits having the bit following highest order bit of logic "1" as a most significant bit of bit string of predetermined number (e.g. col 7 lines 39-68).

Re claim 12, Allred further discloses in Figures 4 and 6 second bit string selecting unit detects highest order bit of logic "1" by decoding digital data (e.g. col. 7 lines 5-15 similarly as seen in selecting position of the first string).

Re claim 13, Allred further discloses in Figures 4 and 6 second bit string extracting unit extracts the bit string of predetermined number of bits including the bit following highest order bit as the most significant bit, based on the result of detection decoded by second bit string selecting unit (e.g. col. 5 lines 30-50 and col. 7 lines 39-68).

Re claim 14, Allred further discloses in Figures 4 and 6 second bit string extracting unit is composed of a switching circuit for extracting the bit string of predetermined number of bits based on the result of detection by second bit string selecting unit (e.g. col. 7 lines 5-15 similarly as seen in selecting position of the first string).

Re claim 15, it is a method claim of claim 1. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,570,310 to Smith discloses a method and data processor for finding a logarithm of a number.

b. U.S. Patent No. 6,587,070 to Hallse discloses a digital base-10 logarithm converter.

c. U.S. Patent No. 5,363,321 to Dao Trong et al. disclose a digital circuit for calculating a logarithm of a number.

d. U.S. Patent No. 4,626,825 to Burleson et al. disclose a logarithmic conversion apparatus.

e. U.S. Patent No. 4,748,577 to Marchant discloses a logarithmic data compression.

f. U.S. Patent No. 6,976,043 to Clifton discloses a technique for approximating functions based on Lagrange polynomials.

g. U.S. Patent No. 5,920,493 to Lau discloses an apparatus and method to determine a most significant bit.

h. U.S. Patent No. 6,711,601 to Inoue et al. disclose a logarithmic arithmetic unit avoiding division as far as predetermined arithmetic precision is guaranteed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

January 8, 2007